IPW

Docket No.: 1309.43490X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

Keishi TAMURA et al.

Serial No. 10/769,805

Filed: February 3, 2004

For: STORAGE SYSTEM AND STORAGE CONTROLLER

SUPPLEMENTAL REQUEST FOR RECONSIDERATION

June 17, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Supplemental to the Request for Reconsideration filed on April 20, 2005, in view of the meeting between Mr. Brundidge and Mr. Laufer held on June 9, 2005 clarifying issues related to the granting of Petitions to Make Special, Applicants submit the following additional remarks.

It is submitted that the cited references, whether considered alone or in combination, fail to disclose or suggest the invention as claimed. In particular, the cited references, at a minimum, fail to disclose or suggest in combination with the other limitations recited in the claims:

a first feature of the present invention as recited in independent claim 1 wherein a first storage controller has at least one or more logical units accessed by a host device, and at least one or more intermediate memory hierarchies arranged so as to

connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies is connected to a memory device arranged in a second storage controller;

a second feature of the present invention as recited in independent claim 2 wherein at least one or more intermediate memory hierarchies arranged so as to connect said logical unit and at least one or more memory devices, and wherein at least one of the intermediate memory hierarchies is connected to the memory device arranged in the second storage controller;

a third feature of the present invention as recited in independent claim 6 including obtaining path information to a memory device arranged in said second storage controller; and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device;

a fourth feature of the present invention as recited in independent claim 7 including obtaining path information to the memory device arranged in said second storage controller; and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device;

a fifth feature of the present invention as recited in independent claim 8 including selecting plural paths connected to said external memory device, reading data from said external memory device through each of these selected paths, and judging whether each of these read data is conformed or not; and

a sixth feature of the present invention as recited in independent claim 9 including selecting plural paths connected to said external memory device, reading data from said external memory device through each of these selected paths, judging

whether each of these read data is conformed or not, writing separate data different from said read data from one of said selected paths when each of the read data is conformed, again reading data from said external memory device through each of said selected paths, and judging whether these read data are conformed to said separate data or not.

To the extent applicable to the present Petition, Applicants submit that although the distinguishing feature(s) may represent a substantial portion of the claimed invention, the claimed invention including said feature(s) and their inter-operation provides a novel storage system and system and method related to or implemented in or by said storage system not taught or suggested by any of the references of record.

The references considered most closely related to the claimed invention are briefly discussed below:

U.S. Patent No. 5,504,882 (Chai et al.) discloses a fault tolerant disk storage subsystem which includes a multipath dynamically alterable hierarchical arrangement of storage device controllers. Multiple storage device controllers are provided which are adapted to emulate a storage device and which each include a cache memory which has multiple data input ports and multiple data output ports. A processing element within the storage device controller is utilized to selectively interconnect particular data input ports with selected data output ports to provide multiple paths within the storage device controller. An interconnection is then provided for coupling a data output port of one or storage device controller with a data input port of one more alternate storage device controllers which emulate storage devices, creating an alterable hierarchical arrangement of storage device controllers. Storage devices are then coupled to each of

the lowest levels of the hierarchical arrangement of storage device controllers. As the storage device controllers may vary in type and capability, various combinations of access speed and redundancy may be provided. Chai et al., at a minimum, fails to disclose or suggest a first storage controller having at least one or more logical units accessed by a host device, and at least one or more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies being connected to a memory device arranged in a second storage controller, and/or obtaining path information to a memory device arranged in said second storage controller, and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device. More particularly, Chai et al. does not disclose or suggest the above described first feature of the present invention as recited in independent claim 1, the above described second feature of the present invention as recited in independent claim 2, the above described third feature of the present invention as recited in independent claim 6, the above described fourth feature of the present invention as recited in independent claim 7, the above described fifth feature of the present invention as recited in independent claim 8 and the above described sixth feature as recited in independent claim 9, in combination with the other limitations recited in each of the independent claims.

U.S. Patent No. 6,073,209 (Bergsten) discloses a computer network comprises a number of storage controllers, each coupled to one of a plurality of storage arrays, each storage array including at least one mass storage device. Each storage controller may be coupled to at least one host processing system and to at least one other

storage controller to control access of the host processing systems to the mass storage devices. Multiple copies of data are maintained in storage arrays that are geographically remote to each other, such that any copy can be accessed by any host. Each storage controllers includes an interface with a host that emulates a mass storage device and an interface with a local storage array that emulates a host. The interfaces to the host and local storage arrays are independent of the type of host or devices in the local storage array. Two or more hosts may be dissimilar to each other, and two or more storage arrays may include dissimilar mass storage devices. Hosts access stored data using virtual addressing. During a data access, the storage controller connected to the accessing host maps a virtual address provided by the host to a real physical location in any of the storage arrays, such that the actual location of the data is transparent to the host. The storage controllers provide automatic back-up and error correction as well as write protection of back-up copies. Bergsten, at a minimum, fails to disclose or suggest a first storage controller having at least one or more logical units accessed by a host device, and at least one or more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies being connected to a memory device arranged in a second storage controller, and/or obtaining path information to a memory device arranged in said second storage controller, and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device. More particularly, Bergsten does not disclose or suggest the above described first feature of the present invention as recited in independent claim 1, the above described second feature of the present invention as recited in

independent claim 2, the above described third feature of the present invention as recited in independent claim 6, the above described fourth feature of the present invention as recited in independent claim 7, the above described fifth feature of the present invention as recited in independent claim 8 and the above described sixth feature as recited in independent claim 9, in combination with the other limitations recited in each of the independent claims.

U.S. Patent No. 6,295,578 (Dimitroff et al.) discloses a cascaded removable media data storage system includes a first level enhanced removable media data storage system controller connected to a host or server computer network. Connected in parallel to the enhanced first level removable media data storage system controller are at least two enhanced second level removable media data storage system controllers. Each enhanced second level removable media data storage system controllers is connected to a mirrored group of removable media data storage units. Dimitroff et al., at a minimum, fails to disclose or suggest a first storage controller having at least one or more logical units accessed by a host device, and at least one or more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies being connected to a memory device arranged in a second storage controller, and/or obtaining path information to a memory device arranged in said second storage controller, and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device. More particularly, Dimitroff et al. does not disclose or suggest the above described first feature of the present invention as recited in independent claim 1, the above described second feature

of the present invention as recited in independent claim 2, the above described third feature of the present invention as recited in independent claim 6, the above described fourth feature of the present invention as recited in independent claim 7, the above described fifth feature of the present invention as recited in independent claim 8 and the above described sixth feature as recited in independent claim 9, in combination with the other limitations recited in each of the independent claims.

U.S. Patent Publication No. 2003/0221077 (Ohno et al.) discloses a method for controlling a storage system including a host computer, and a first and a second storage control apparatuses each receiving a data input/output request from the host computer and executing a data input/output process for a storage device in response to the request, comprises connecting a first communication path between the host computer and the first apparatus; connecting a second communication path between the first apparatus and the second apparatus; receiving by the first apparatus a first data input/output request from the host computer through the first path; when the first apparatus has judged that the first request is not for the first apparatus, transmitting by the first apparatus a second data input/output request corresponding to the first request, to the second apparatus through the second path; and by the second apparatus, receiving the second request and executing a data input/output process corresponding to the second request received. Ohno et al., at a minimum, fails to disclose or suggest a first storage controller having at least one or more logical units accessed by a host device, and at least one or more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies being connected to a memory device arranged in

a second storage controller, and/or obtaining path information to a memory device arranged in said second storage controller, and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device. More particularly, Ohno et al. does not disclose or suggest the above described first feature of the present invention as recited in independent claim 1, the above described second feature of the present invention as recited in independent claim 2, the above described third feature of the present invention as recited in independent claim 6, the above described fourth feature of the present invention as recited in independent claim 7, the above described fifth feature of the present invention as recited in independent claim 8 and the above described sixth feature as recited in independent claim 9, in combination with the other limitations recited in each of the independent claims.

Therefore, since the cited references fail to disclose or suggest the above described first feature of the present invention as recited in independent claim 1, the above described second feature of the present invention as recited in independent claim 2, the above described third feature of the present invention as recited in independent claim 6, the above described fourth feature of the present invention as recited in independent claim 7, the above described fifth feature of the present invention as recited in independent claim 8 and the above described sixth feature as recited in independent claim 9, in combination with the other limitations recited in each of the independent claims, it is submitted that all of the claims are patentable over the cited references whether said references are taken individually or in combination with each other.

In view of the foregoing, Applicant requests that this Petition to Make Special be granted and that the application undergo the accelerated examination procedure set forth in MPEP 708.02 VIII.

Respectfully submitted,

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